ECS - TE sem VI Reg C'scheme Summer 2025 14/5/2025

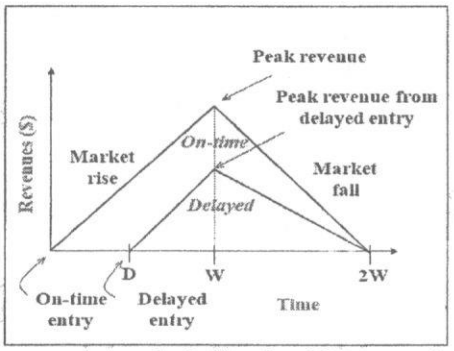
(3 Hours) [Total Marks: 80]

N.B.: (1) Question No. 1 is **Compulsory**.
(2) Attempt any **three** questions out of the remaining **five**.
(3) Each question carries 20 marks and sub-question carry equal marks.
(4) Assume suitable data if required.

1. Solve **any 4**
   (a) Describe features of ARM Cortex M3 **(5)**
   (b) Explain the conditions which give rise to Deadlock condition. **(5)**
   (c) Draw control flow graph for finding the roots of quadratic equation $X^2+4X+4=0$ **(5)**
   (d) Discuss requirement of hardware testing and software testing for any one embedded system of your choice. **(5)**
   (e) Elaborate effect of priority inversion in real time systems. **(5)**

2. (a) Explain with neat diagram, Memory map and the bus interface of ARM Cortex M3 microcontroller. **(10)**
   (b) Decide whether the tasks are schedulable by Necessary and sufficient condition in an embedded system with 4 different tasks with task IDs T1, T2, T3, T4, T5 and estimated completion time 2.3,3,5,1.5 and 3.25 mS respectively. T1, T2, T3, T4 and T5 have their cycle duration as 25, 30, 50, 40 and 35 ms respectively. **(10)**

3. (a) **(10)**



Explain the terms and their significance shown in above diagram with respect to embedded system.
   (b) Explain the difference between the ARM, Thumb and Thumb 2 mode of operations in ARM Cortex M3? **(10)**

4. (a) List and explain any four common RTOS kernel objects with an example each. **(10)**
   (b) Summarize the differences in the operation of RS232 and RS485 **(10)**

5 (a) Examine the statement, "Optimizing design metrics is a key challenge" **(10)**
   (b) Examine the fundamental issues in hardware and software co-design. **(10)**

6. Illustrate waterfall model use in the product design cycle of any one embedded system from following: 1) Pace maker 2) Missile launching system 3) Air bag control system in 4-wheeler 4) Microwave oven **(20)**
